# Computing Architectures based on the Human Auditory Pathway

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Lloyd Watts

Founder and Chief Scientist, Audience



## DARPA / IARPA / NICE:

- Brains can solve real-world problems that computers can't yet solve (noisy, ambiguous inputs, incomplete data)
  - What algorithms / software architectures can we design to match human performance?
- Brains can solve those problems at vastly lower power consumption than modern PCs (~250 W for ~16 GFlops) or High-Performance Computers (~30 MW(?) for ~17.6 PetaFlops)
  - What hardware architectures or components can allow us to reach brain-like efficiency?

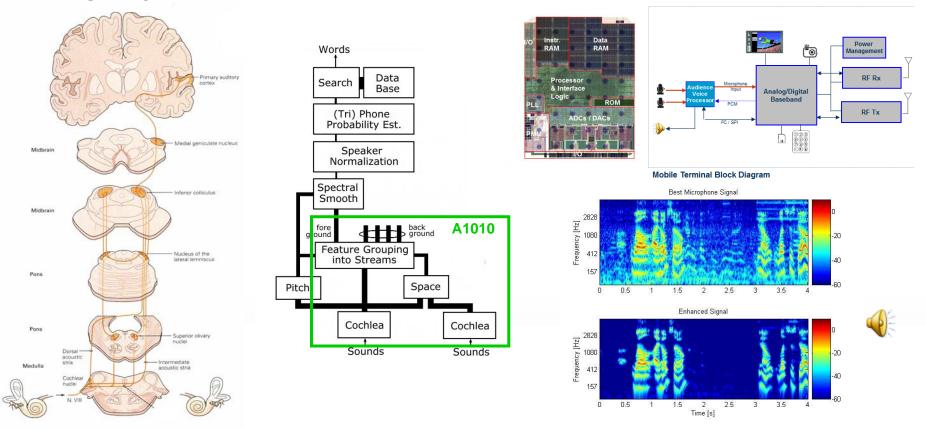
### **Audience Introduction**

#### • Founded in 2000, Mission:

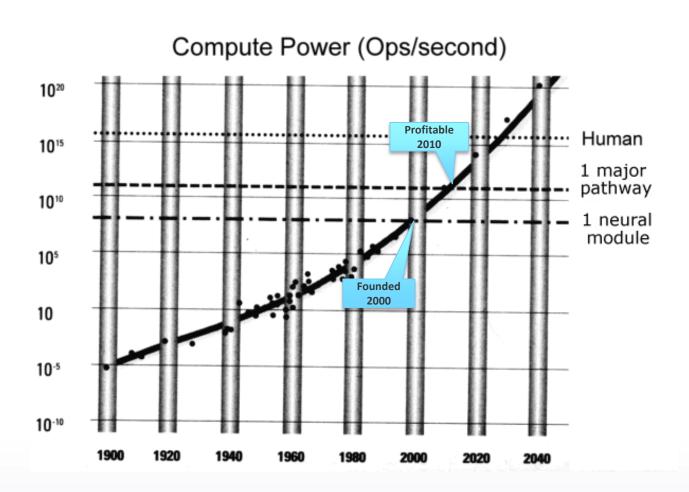
- Reverse Engineer the Human Hearing System
- Commercialize with dedicated chip products

#### • First Product:

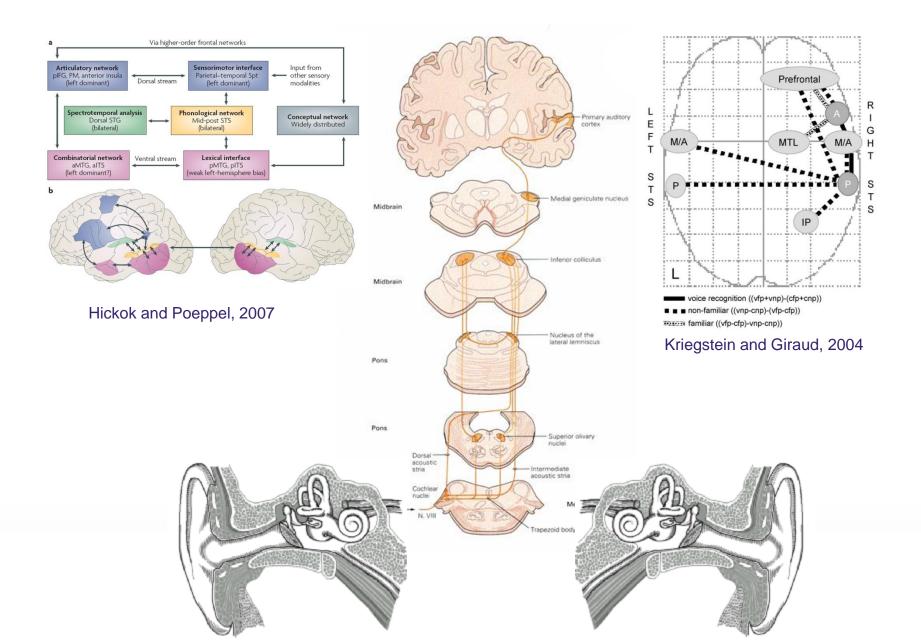
 2-microphone Noise Reduction Chip for Cell Phones, offered in 2007, Hit in 2010, IPO in 2012

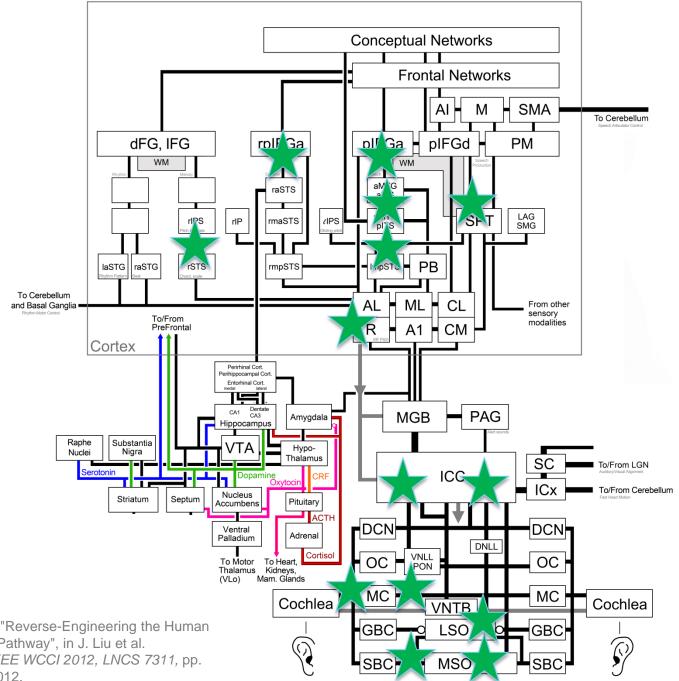


## Timing is Everything



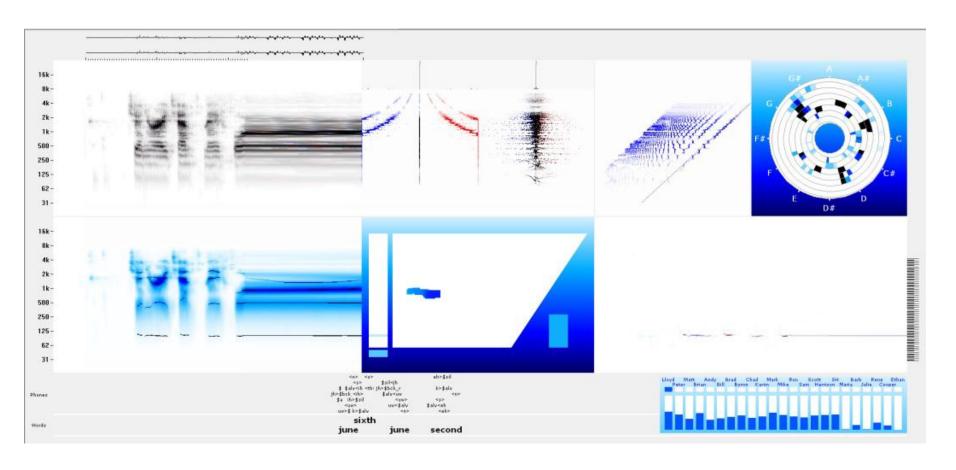
#### The Auditory Pathway (as seen in 2012)





L. Watts, "Reverse-Engineering the Human Auditory Pathway", in J. Liu et al. (Eds.): IEEE WCCI 2012, LNCS 7311, pp. 47-59, 2012.

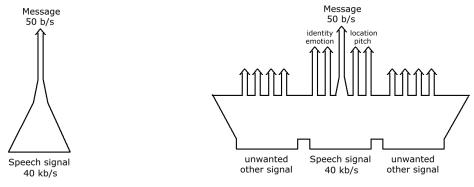
### Real-Time Multi-Representation Working Model



L. Watts, "Reverse-Engineering the Human Auditory Pathway", in J. Liu et al. (Eds.): *IEEE WCCI 2012, LNCS 7311,* pp. 47–59, 2012.

### **Brain-Like Software Architectures**

- Brains use high-resolution representations of the world, computed in realtime with low latency
- Many derived representations are computed from raw signals to get a final high-quality answer



- Neuroscience advisors steered me away from spiking representations
- Many different algorithms appear to be running in cortex (associative memory, HMM/Viterbi Search, Pattern Match, etc.) – not just one algorithm (FOXP2 gene as example)
- Neuroscience knowledge has been keeping up with computing capability as hoped in 2000, computing capability keeps advancing (so far)
- Intel has been keeping up for my simulations core i7, Xeon Phi. Haven't needed (or been able to exploit) GPU yet

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# Brain-Like Hardware Architectures for Low-Power SuperComputing

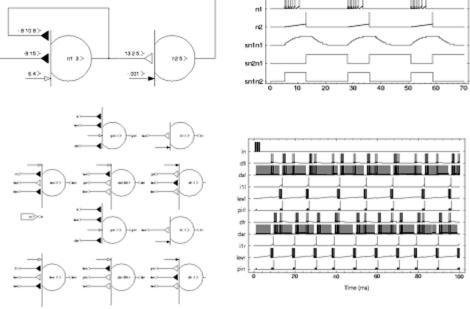
- P = N C V<sup>2</sup> f
- Many computing elements (large N), running very slow (f = 1 kHz) which leads to small V (85 mV)
- Special-purpose hardware to implement important, often-used functions (i.e. auditory brainstem).
- Careful power supply management only activate domain when needed
- This requires MUCH MORE HARDWARE, in a tight space (sphere, block).
  - e.g. cell-phone noise reduction chip (20mW, 100MHz, 4mm<sup>2</sup>, \$1)
  - vs. hearing Aid chip (0.5mW, 20MHz, 20mm<sup>2</sup>, \$10)
- A Modest Proposal: Imagine a 1kg 3D block of silicon (or stacks of chips, all with 10 kHz clocks, each consuming microWatts of power).
  - Much more silicon, therefore very expensive and heavy (like the brain)!
  - But much less cost for heat-sinks, much less air conditioning
- <u>Don't have to abandon digital processing</u> to get very low power. We would have to really embrace parallelism and low-power design at very high cost in low volumes, suggesting a government funding reason to pursue it (i.e. commercial forces very unlikely to get us there).

## PostScript: Event-Driven Simulation of Networks of Spiking Neurons

- After the group discussion, it seemed like this subject may be of interest to some attendees:
- http://www.lloydwatts.com/spike2.html
- L. Watts, "Event-Driven Simulation of Networks of Spiking Neurons", *Proceedings of the Sixth Neural Information Processing Systems Conference*, 1993, pp. 927-934.
- Examples of the Spike simulator:

Tonic Burster with Ca++ adaptation

Locust Walking Circuit



## Thank you!

www.audience.com

www.lloydwatts.com